

# Advanced Regulating Pulse Width Modulators

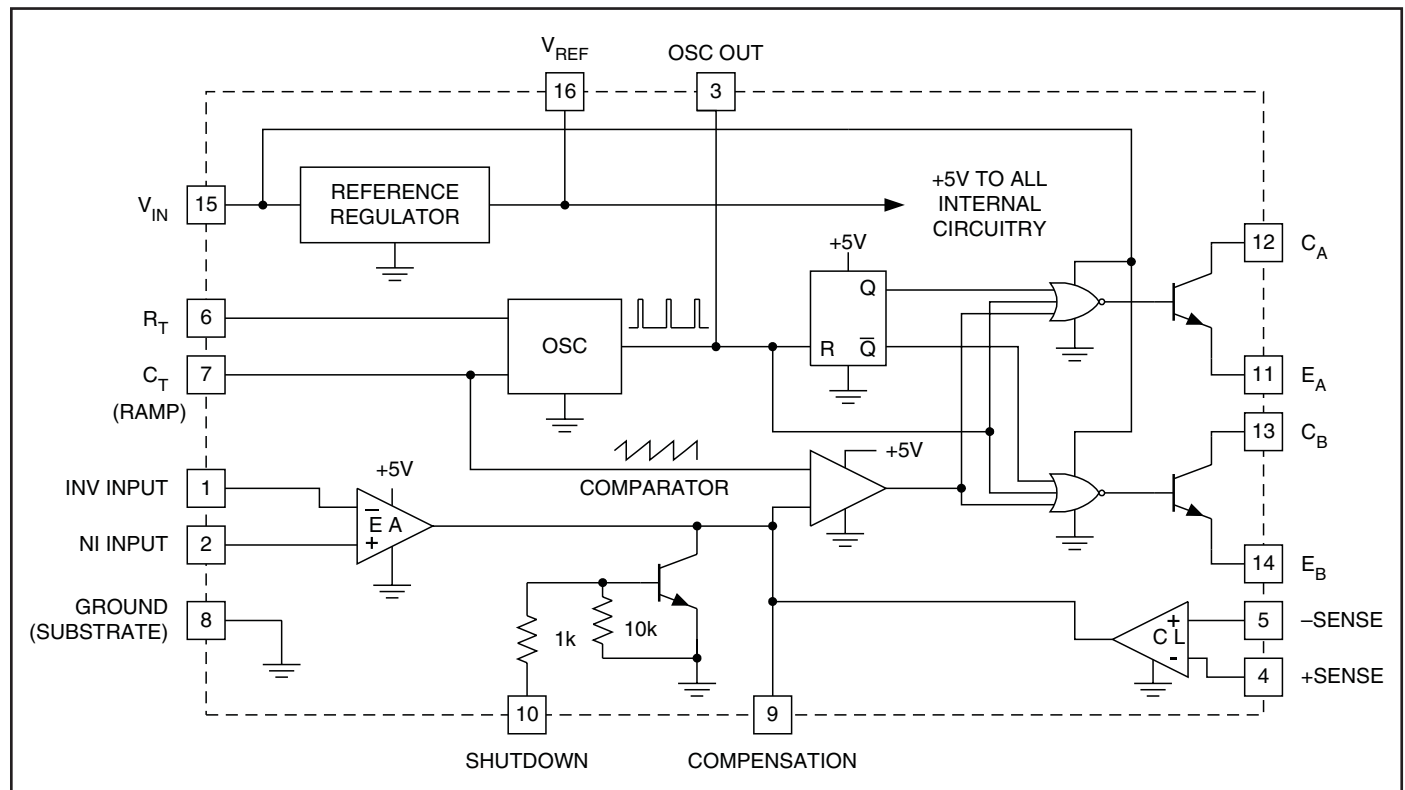
## FEATURES

- Complete PWM Power Control Circuitry
- Uncommitted Outputs for Single-ended or Push-pull Applications
- Low Standby Current...8mA Typical
- Interchangeable with SG1524, SG2524 and SG3524, Respectively

## DESCRIPTION

The UC1524, UC2524 and UC3524 incorporate on a single monolithic chip all the functions required for the construction of regulating power supplies, inverters or switching regulators. They can also be used as the control element for high-power-output applications. The UC1524 family was designed for switching regulators of either polarity, transformer-coupled dc-to-dc converters, transformerless voltage doublers and polarity converter applications employing fixed-frequency, pulse-width modulation techniques. The dual alternating outputs allow either single-ended or push-pull applications. Each device includes an on-chip reference, error amplifier, programmable oscillator, pulse-steering flip-flop, two uncommitted output transistors, a high-gain comparator, and current-limiting and shut-down circuitry. The UC1524 is characterized for operation over the full military temperature range of -55°C to +125°C. The UC2524 and UC3524 are designed for operation from -25°C to +85°C and 0° to +70°C, respectively.

## BLOCK DIAGRAM



## ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage,  $V_{CC}$  (Notes 2 and 3) . . . . . 40V  
Collector Output Current . . . . . 100mA  
Reference Output Current . . . . . 50mA  
Current Through  $C_T$  Terminal . . . . . -5mA  
Power Dissipation at  $T_A = +25^\circ\text{C}$  (Note 4) . . . . . 1000mW  
Power Dissipation at  $T_C = +25^\circ\text{C}$  (Note 4) . . . . . 2000mW  
Operating Junction Temperature Range . . . . -55°C to +150°C  
Storage Temperature Range . . . . . -65°C to +150°C

Note 1: Over operating free-air temperature range unless otherwise noted.

Note 2: All voltage values are with respect to the ground terminal, pin 8.

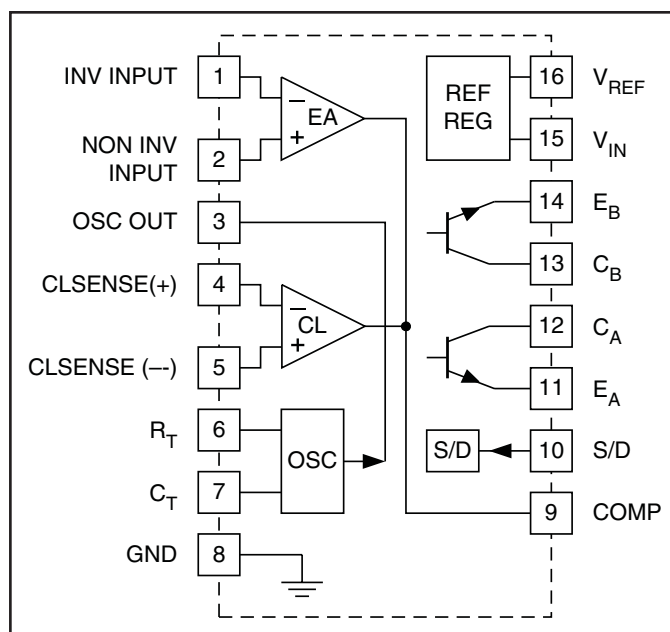
Note 3: The reference regulator may be bypassed for operation from a fixed 5V supply by connecting the  $V_{CC}$  and reference output pins both to the supply voltage. In this configuration the maximum supply voltage is 6V.

Note 4: Consult packaging section of databook for thermal limitations and considerations of package.

## RECOMMENDED OPERATING CONDITIONS

Supply Voltage,  $V_{CC}$  . . . . . 8V to 40V  
Reference Output Current . . . . . 0 to 20mA  
Current through  $C_T$  Terminal . . . . . -0.03mA to -2mA  
Timing Resistor,  $R_T$  . . . . . 1.8k $\Omega$  to 100k $\Omega$   
Timing Capacitor,  $C_T$  . . . . . 0.001 $\mu\text{F}$  to 0.1 $\mu\text{F}$   
Operating Ambient Temperature Range  
UC1524 . . . . . -55°C to +125°C  
UC2524 . . . . . -25°C to +85°C  
UC3524 . . . . . 0°C to +70°C

## CONNECTION DIAGRAM



**ELECTRICAL CHARACTERISTICS:** Unless otherwise stated, these specifications apply for  $T_A = -55^\circ\text{C}$  to  $+125^\circ\text{C}$  for the UC1524,  $-25^\circ\text{C}$  to  $+85^\circ\text{C}$  for the UC2524, and  $0^\circ\text{C}$  to  $+70^\circ\text{C}$  for the UC3524,  $V_{IN} = 20\text{V}$ , and  $f = 20\text{kHz}$ ,  $T_A = T_J$ .

PARAMETER	TEST CONDITIONS	UC1524/UC2524			UC3524			UNITS
		MIN		MAX	MIN		MAX	
Reference Section								
Output Voltage		4.8	5.0	5.2	4.6	5.0	5.4	V
Line Regulation	V <sub>IN</sub> = 8 to 40V		10	20		10	30	mV
Load Regulation	I <sub>L</sub> = 0 to 20mA		20	50		20	50	mV
Ripple Rejection	f = 120Hz, T <sub>J</sub> = 25°C		66			66		dB
Short Circuit Current Limit	V <sub>REF</sub> = 0, T <sub>J</sub> = 25°C		100			100		mA
Temperature Stability	Over Operating Temperature Range		0.3	1		0.3	1	%
Long Term Stability	T <sub>J</sub> = 125°C, t = 1000 Hrs.		20			20		mV
Oscillator Section								
Maximum Frequency	C <sub>T</sub> = .001mfd, R <sub>T</sub> = 2kΩ		300			300		kHz
Initial Accuracy	R <sub>T</sub> and C <sub>T</sub> Constant		5			5		%
Voltage Stability	V <sub>IN</sub> = 8 to 40V, T <sub>J</sub> = 25°C			1			1	%
Temperature Stability	Over Operating Temperature Range			5			5	%
Output Amplitude	Pin 3, T <sub>J</sub> = 25°C		3.5			3.5		V
Output Pulse Width	C <sub>T</sub> = .01mfd, T <sub>J</sub> = 25°C		0.5			0.5		μs
Error Amplifier Section								
Input Offset Voltage	V <sub>CM</sub> = 2.5V		0.5	5		2	10	mV
Input Bias Current	V <sub>CM</sub> = 2.5V		2	10		2	10	μA
Open Loop Voltage Gain		72	80		60	80		dB
Common Mode Voltage	T <sub>J</sub> = 25°C	1.8		3.4	1.8		3.4	V

**ELECTRICAL CHARACTERISTICS:** Unless otherwise stated, these specifications apply for  $T_A = -55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  for the UC1524,  $-25^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  for the UC2524, and  $0^{\circ}\text{C}$  to  $+70^{\circ}\text{C}$  for the UC3524,  $V_{IN} = 20\text{V}$ , and  $f = 20\text{kHz}$ ,  $T_A = T_J$ .

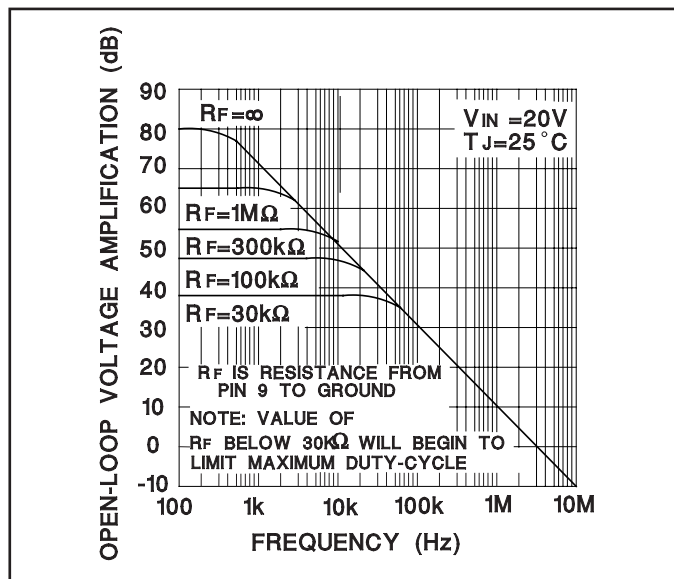
PARAMETER	TEST CONDITIONS	UC1524/UC2524			UC3524			UNITS
		MIN		MAX	MIN		MAX	
Error Amplifier Section (cont.)								
Common Mode Rejection Ratio	T <sub>J</sub> = 25°C		70			70		dB
Small Signal Bandwidth	A <sub>v</sub> = 0dB, T <sub>J</sub> = 25°C		3			3		MHz
Output Voltage	T <sub>J</sub> = 25°C	0.5		3.8	0.5		3.8	V
Comparator Section								
Duty-Cycle	% Each Output On	0		45	0		45	%
Input Threshold	Zero Duty-Cycle		1			1		V
	Maximum Duty-Cycle		3.5			3.5		V
Input Bias Current			1			1		μA
Current Limiting Section								
Sense Voltage	Pin 9 = 2V with Error Amplifier Set for Maximum Out, T <sub>J</sub> = 25°C	190	200	210	180	200	220	mV
Sense Voltage T.C.			0.2			0.2		mV/°C
Common Mode Voltage	T <sub>J</sub> = -55°C to 85°C for the -1V to 1V Limit	-1		+1	-1		+1	V
	T <sub>J</sub> = 125°C	-0.3		+1				V
Output Section (Each Output)								
Collector-Emitter Voltage		40			40			V
Collector Leakage Current	V <sub>CE</sub> = 40V		0.1	50		0.1	50	μA
Saturation Voltage	I <sub>C</sub> = 50mA		1	2		1	2	V
Emitter Output Voltage	V <sub>IN</sub> = 20V	17	18		17	18		V
Rise Time	R <sub>C</sub> = 2kΩ, T <sub>J</sub> = 25°C		0.2			0.2		μs
Fall Time	R <sub>C</sub> = 2kΩ, T <sub>J</sub> = 25°C		0.1			0.1		μs
Total Standby Current (Note)	V <sub>IN</sub> = 40V		8	10		8	10	mA

## PRINCIPLES OF OPERATION

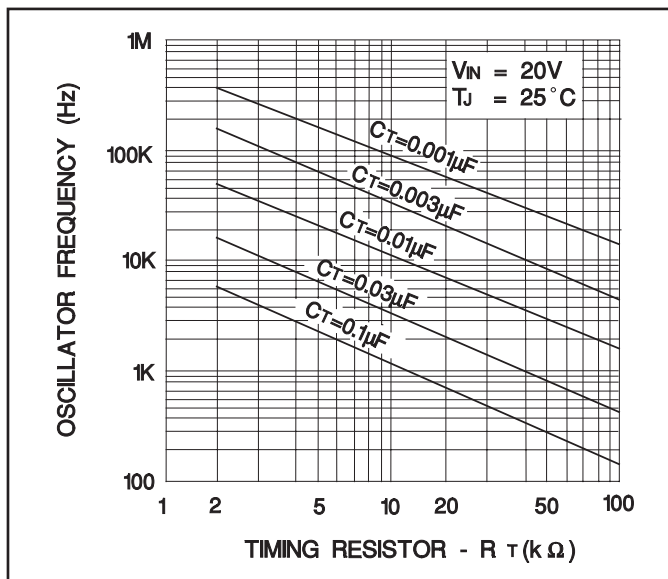
The UC1524 is a fixed-frequency pulse-width-modulation voltage regulator control circuit. The regulator operates at a frequency that is programmed by one timing resistor ( $R_T$ ), and one timing capacitor ( $C_T$ ).  $R_T$  establishes a constant charging current for  $C_T$ . This results in a linear voltage ramp at  $C_T$ , which is fed to the comparator providing linear control of the output pulse width by the error amplifier. The UC1524 contains an on-board 5V regulator that serves as a reference as well as powering the UC1524's internal control circuitry and is also useful in supplying external support functions. This reference voltage is lowered externally by a resistor divider to provide a reference within the common-mode range of the error amplifier or an external reference may be used. The power supply output is sensed by a second resistor divider network to generate a feedback signal to the error amplifier. The amplifier output voltage is then compared to the linear voltage ramp at  $C_T$ . The resulting modulated pulse out of the high-gain comparator is then steered to

the appropriate output pass transistor ( $Q_1$  or  $Q_2$ ) by the pulse-steering flip-flop, which is synchronously toggled by the oscillator output. The oscillator output pulse also serves as a blanking pulse to assure both outputs are never on simultaneously during the transition times. The width of the blanking pulse is controlled by the value of  $C_T$ . The outputs may be applied in a push-pull configuration in which their frequency is half that of the base oscillator, or paralleled for single-ended applications in which the frequency is equal to that of the oscillator. The output of the error amplifier shares a common input to the comparator with the current limiting and shutdown circuitry and can be overridden by signals from either of these inputs. This common point is also available externally and may be employed to control the gain of, or to compensate, the error amplifier or to provide additional control to the regulator.

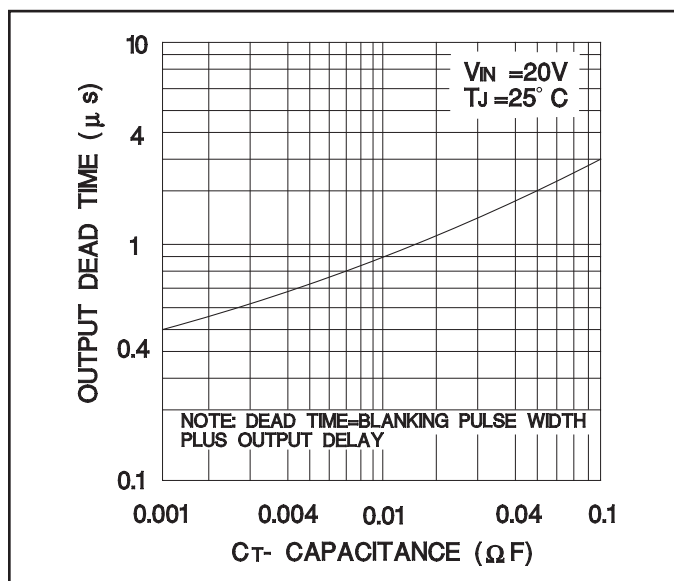
## TYPICAL CHARACTERISTICS



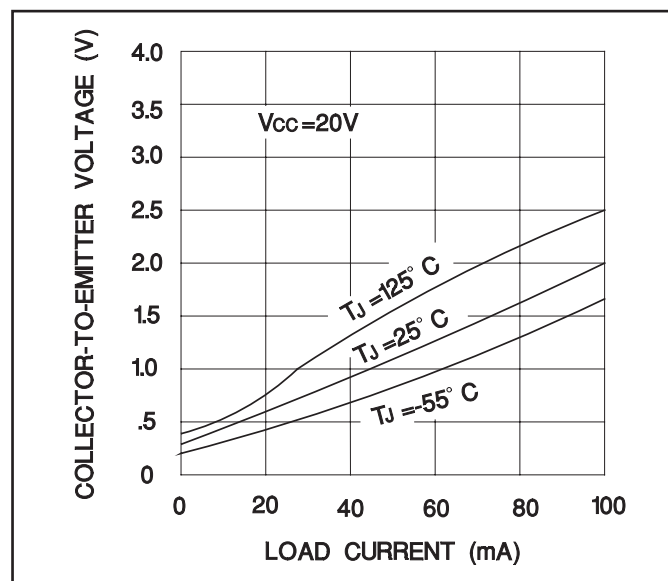
Open-loop voltage amplification of error amplifier vs frequency.



Oscillator frequency vs timing components.



Output dead time vs timing capacitance value.



Output saturation voltage vs load current.



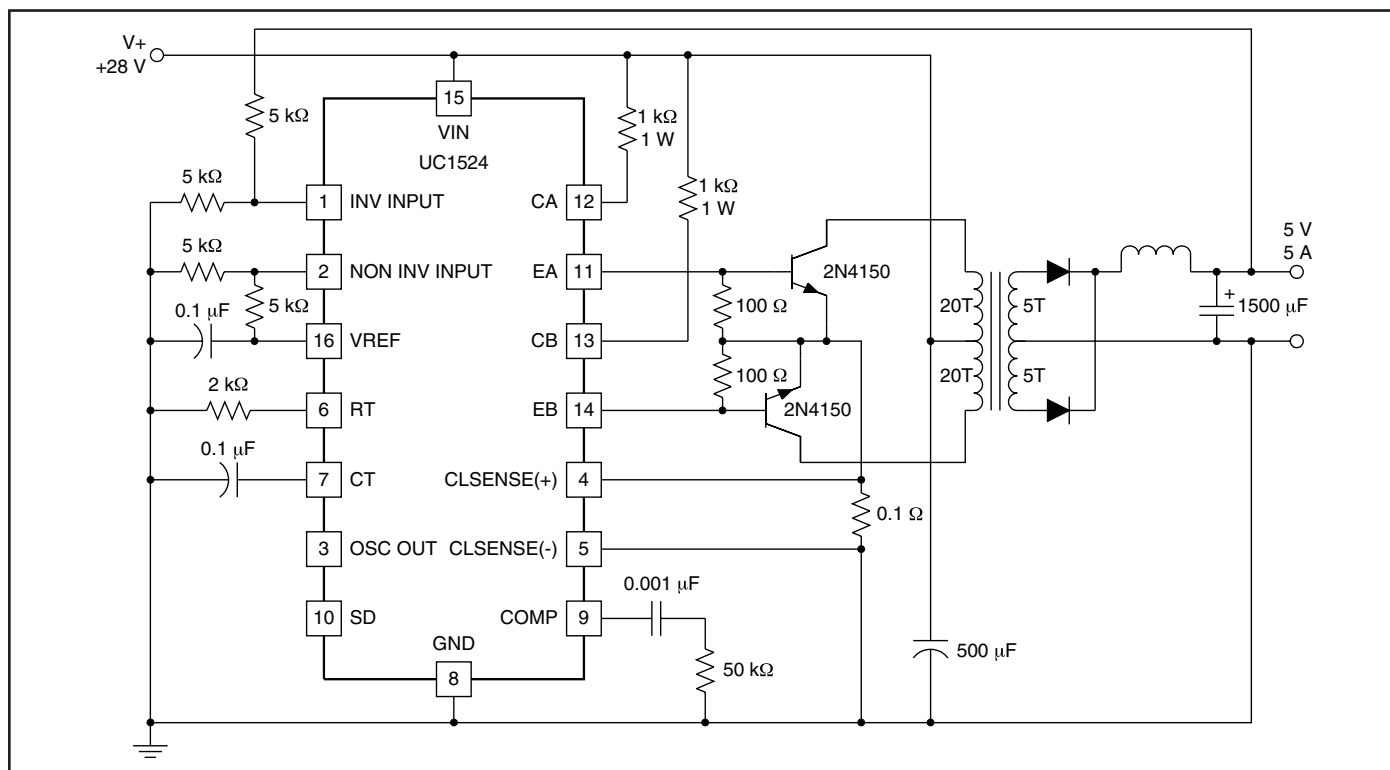


Figure 3. Push-pull transformer coupled circuit.

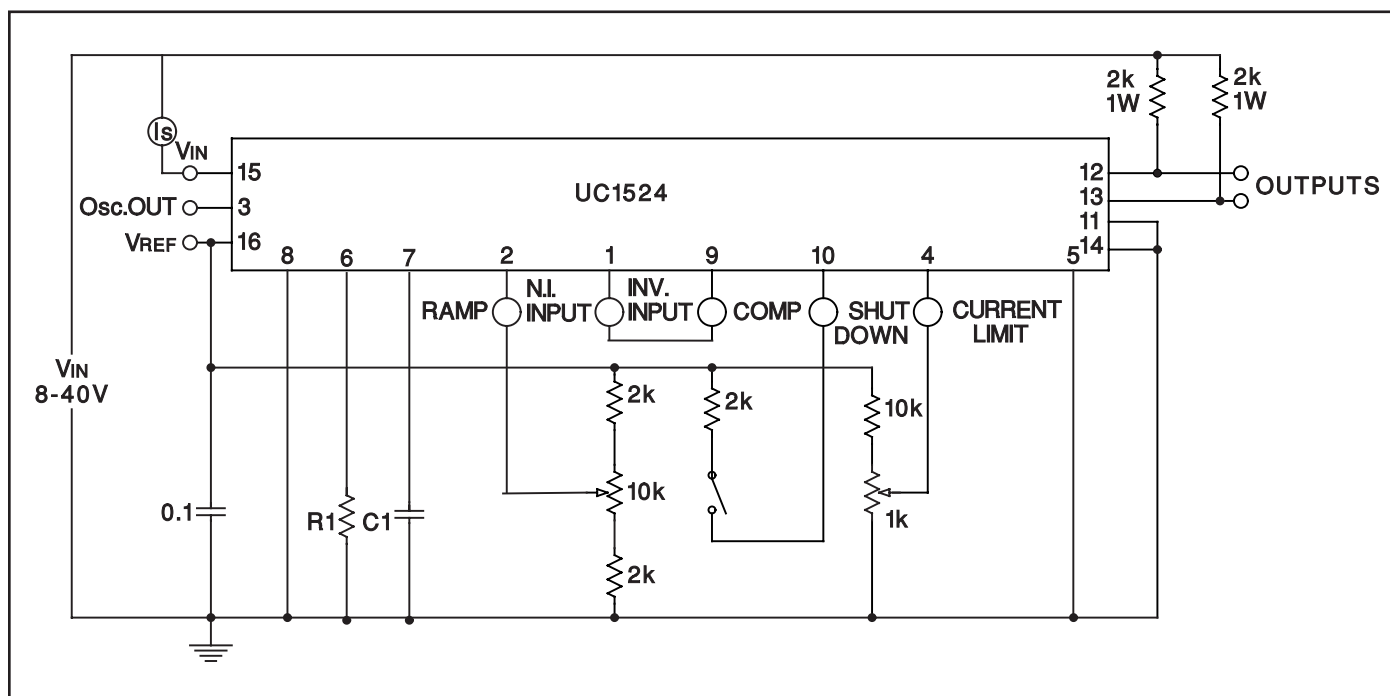


Figure 4. Open loop test circuit.

## PACKAGING INFORMATION

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
UC1524J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI
UC1524J/80937	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI
UC1524J883B	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI
UC2524DW	ACTIVE	SOIC	DW	16	40	TBD	CU NIPDAU	Level-2-220C-1 YEAR
UC2524DWTR	ACTIVE	SOIC	DW	16	2000	TBD	CU NIPDAU	Level-2-220C-1 YEAR
UC2524J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI
UC2524N	ACTIVE	PDIP	N	16	25	TBD	CU NIPDAU	Level-NA-NA-NA
UC3524D	ACTIVE	SOIC	D	16	40	TBD	CU NIPDAU	Level-1-220C-UNLIM
UC3524DTR	ACTIVE	SOIC	D	16	2500	TBD	CU NIPDAU	Level-1-220C-UNLIM
UC3524DW	ACTIVE	SOIC	DW	16	40	TBD	CU NIPDAU	Level-2-220C-1 YEAR
UC3524DWTR	ACTIVE	SOIC	DW	16	2000	TBD	CU NIPDAU	Level-2-220C-1 YEAR
UC3524J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI
UC3524N	ACTIVE	PDIP	N	16	25	TBD	CU NIPDAU	Level-NA-NA-NA

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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J (R-GDIP-T\*\*)

14 LEADS SHOWN

# CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.



## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



14/18 Pin Only  
20 Pin vendor option

4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

## D (R-PDSO-G16)

## PLASTIC SMALL-OUTLINE PACKAGE



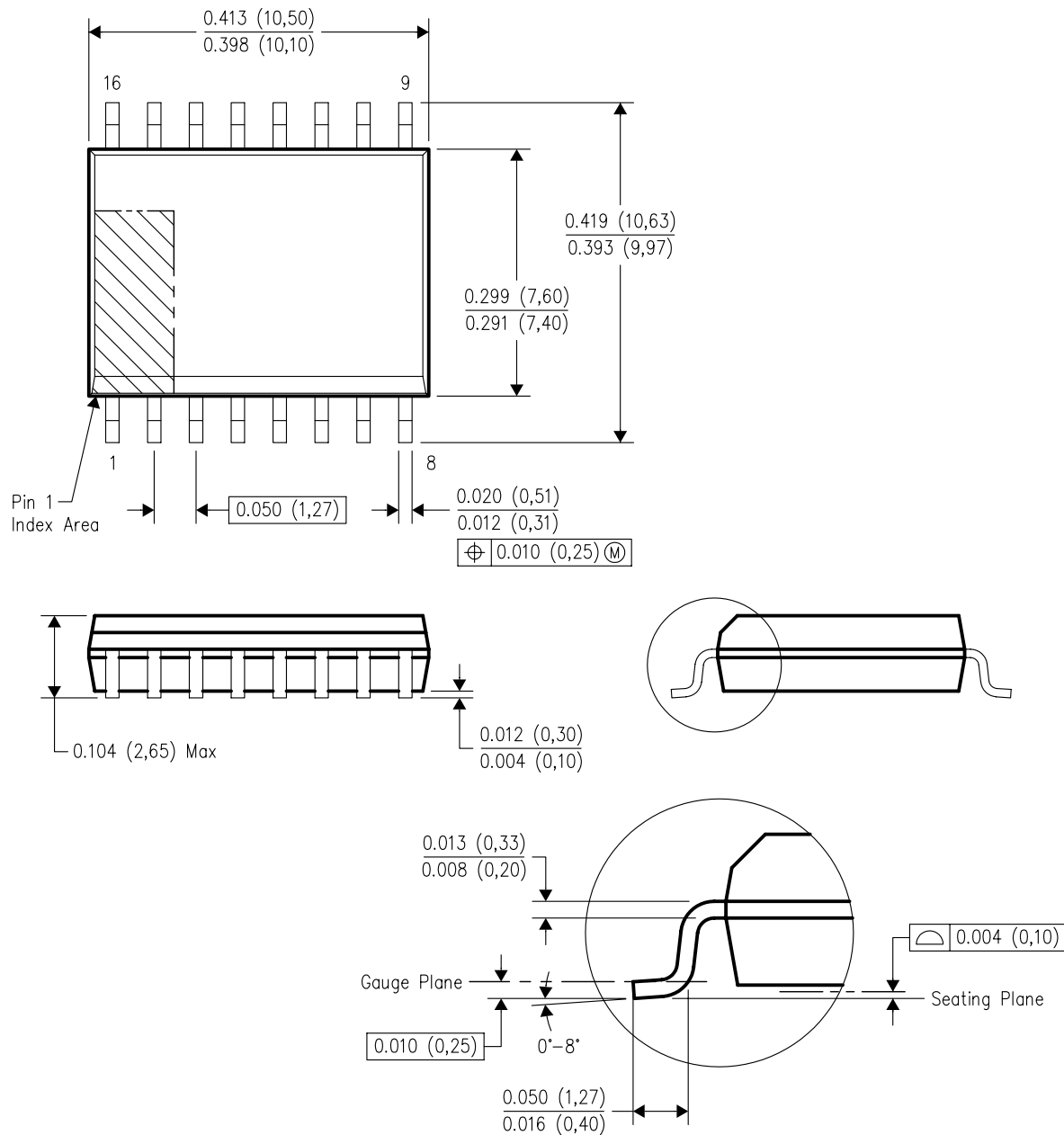
4040047-4/F 07/2004

## NOTES:

- All linear dimensions are in inches (millimeters).
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- Falls within JEDEC MS-012 variation AC.

## DW (R-PDSO-G16)

## PLASTIC SMALL-OUTLINE PACKAGE



4040000-2/F 06/2004

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed  $0.006 (0,15)$ .
  - D. Falls within JEDEC MS-013 variation AA.

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